

Docket No.: P2001,0216



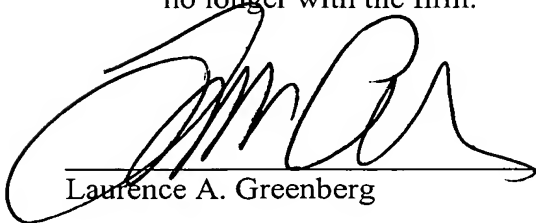
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applic. No. : 10/673,705 Confirmation No.: 2451
Inventor : Annalisa Cappellani et al.
Filed : September 26, 2003
TC/A.U. : 2829
Examiner : Scott B. Geyer

DECLARATION TO ACCOMPANY
PETITION UNDER 37 C.F.R. 1.8(b) and 1.10(c)

I, Laurence A. Greenberg, hereby declare that:

- ❖ to the best of my knowledge and belief, the mailing of September 26, 2003 was sent by Express Mail to the Patent and Trademark Office on that date;
- ❖ to the best of my knowledge and belief, the mailing of October 23, 2003, was sent by first class mail to the Patent and Trademark Office on that date;
- ❖ I have reviewed the pertinent pages of the outgoing mail log for September 26, 2003, and October 23, 2003, and the pages show that the papers as listed in the accompanying amendment were indeed mailed on the dates indicated above;
- ❖ the mailing of October 23, 2003 was originally signed by Mark Weichselbaum who is no longer with the firm.



Laurence A. Greenberg

LAURENCE A. GREENBERG
REG. NO. 29,308

Date:

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Date of Deposit September 26, 2003

I hereby certify that this paper or fee is being deposited with the United States Postal Service
"Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and
is addressed to the Commissioner for Patents, Alexandria, VA 22313-1450.

Docket No.: P2001,0216


MICHAEL BURNS

Date: September 26, 2003

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed herewith are the necessary papers for filing the following application for
Letters Patent:

Applicant : ANNALISA CAPPELLANI ET AL.

Title : METHOD FOR FABRICATING A MOSFET HAVING A VERY
SMALL CHANNEL LENGTH

1 sheet of drawings.

The payment in the amount of \$750.00 covering the filing fee.

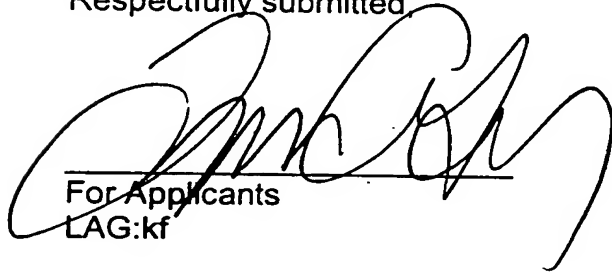
PCT Cover Sheet WO 02/078058 A2

Information Disclosure Statement and 15 References.

This application is being filed without a signed oath or declaration under the
provisions of 37 CFR 1.53(f). Applicants await notification of the date by which the
oath or declaration and the surcharge are due, pursuant to this rule.

The Patent and Trademark Office is hereby given authority to charge Deposit Account No. 12-1099 of Lerner and Greenberg, P.A. for any fees due or deficiencies of payments made for any purpose during the pendency of the above-identified application.

Respectfully submitted



For Applicants
LAG:kf

LAURENCE A. GREENBERG
REG. NO. 29,308



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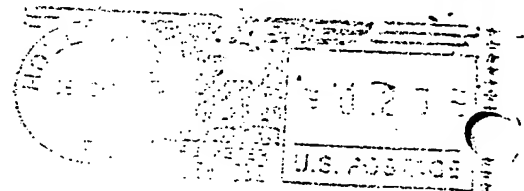
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DOCKET NO. P2001,0216..... Mailed September 26, 2003

APPLIC. NO. Express Mail EV 309760700 US.

The stamp of the Patent Office hereon may be considered the date on which paper indicated below were received.

Applic pgs... Rule 53b New ☒ Contin ☐ Div ☐ CIP ☐ / Rule 53c Prov. ☐ / Rule 53d CPA... RCE ☐
☐ CIP... pgs ☐ Design ☒ I. Dwgs ☐ Declaration ☒ Mailing Certif.
☐ Priority Claim ☐ Cert. Prior. Doc(s) ☒ PCT Cover Sheet WO 02/1018058
☐ Amend pgs... ☐ Prel. Amend pgs... ☐ Letter
☐ Response pgs... ☐ 37CFR1.116 ☐ Not. of Appeal
☐ Brief pgs... ☐ Appndx pgs... ☒ I.D.S. + 15 Refs.
☐ Assoc Pwr of Atty ☒ Credit Card \$ 750.00
☐ Pet. for Ext.... Mo. ☐ Pet.... ☐ Check \$....
☐ Issue Fee ☐ Assignment ☒ PTOL 14.49.
☐ Cert. Trans. ☐ Cert. of Corr. ☐ File rec. corr
Intern Search Report

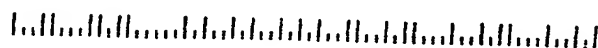
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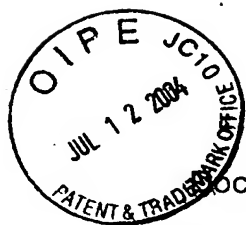
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Hollywood, FL 33022-2480

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ocket No.: P2001,0216

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : ANNALISA CAPPELLANI ET AL.
Filed : CONCURRENTLY HEREWITH
Title : METHOD FOR FABRICATING A MOSFET HAVING A VERY
SMALL CHANNEL LENGTH

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 6,091,120 (Yeom et al.), dated July 18, 2000;

U.S. Patent No. 5,089,863 (Sato et al.), dated February 18, 1992;

U.S. Patent No. 5,384,479 (Taniguchi), dated January 24, 1995, and corresponding German Patent DE 42 34 528 C2 (Taniguchi), dated April, 15, 1993;

German Published Non-Prosecuted Patent Application DE 42 34 777 A1 (König et al.), dated April 21, 1994, and English abstract thereof;

French Patent Application FR 2 791 177 A1 (Thomas et al.), dated September 22, 2000, and English abstract thereof;

Patent Abstracts of Japan 63044768 (Shinichi), dated February 25, 1988;

European Patent Application EP 0 740 334 A2 (Eckstein et al.), dated October 30, 1996;

European Patent Application EP 0 328 350 A2 (Nakamura et al.), dated August 16, 1989;

PCT WO 02/41383 A1 (Furukawa et al.), dated May 23, 2002;

Widmann, D. et al.: "Technologie hochintegrierter Schaltungen" [Technology of High-Density Integrated Circuits], Springer Verlag, 2nd Edition, pp. 201-203;

Ghani, T. et al.: "100nm Gate Length High Performance/Low Power CMOS Transistor Structure", IEEE, 1999, pp. 415-418;

Lasky, J. B. et al.: "Comparison of Transformation to Low-Resistivity Phase and Agglomeration of TiSi_2 and CoSi_2 ", IEEE Transactions on Electron Devices, Vol. 38, No. 2, February 1991, pp. 262-269;

Hisamoto, D. et al.: "A Low-Resistance Self-Aligned T-Shaped Gate for High-Performance Sub-0.1- μm CMOS", IEEE Transactions on Electron Devices, Vol. 44, No. 6, June 1997, pp. 951-956;

Kasai, K. et al.: "W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs", IEEE, 1994, pp. 497-500;

International Search Report, dated April 14, 2003.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,



For Applicants

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FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEINFORMATION DISCLOSURE
STATEMENT BY APPLICANT
(37 CFR 1.98(b))Attorney Docket No.: P2001,0216
Appl. No.:

Applicant: ANNALISA CAPPELLANI ET AL.

Filing Date: September 26, 2003
Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	6,091,120	7/18/00	Yeom et al.			
	B	5,089,863	2/18/92	Satoh et al.			
	C	5,384,479	1/24/95	Taniguchi			
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
	J	42 34 528 C2	4/15/93	Germany			
	K	42 34 777 A1	4/21/94	Germany			
	L	2 791 177 A1	9/22/00	France			
	M	63044768	2/25/88	Japan			
	N	0 740 334 A2	10/30/96	Europe			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Widmann, D. et al.: "Technologie hochintegrierter Schaltungen" [Technology of High-Density Integrated Circuits], Springer Verlag, 2 nd Edition, pp. 201-203
		Ghani, T. et al.: "100nm Gate Length High Performance/Low Power CMOS Transistor Structure", IEEE, 1999, pp. 415-418

EXAMINER

DATE CONSIDERED



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STATEMENT BY APPLICANT
(37 CFR 1.98(b))Attorney Docket No.: P2001,0216
Appl. No.:Applicant: ANNALISA CAPPELLANI ET
AL.Filing Date: September 26, 2003
Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
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FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
	J	0 328 350 A2	8/16/89	Europe			
	K	02/41383 A1	5/23/02	WIPO			
	L						
	M						
	N						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Lasky, J. B. et al.: "Comparison of Transformation to Low-Resistivity Phase and Agglomeration of TiSi_2 and CoSi_2 ", IEEE Transactions on Electron Devices, Vol. 38, No. 2, February 1991, pp. 262-269
		Hisamoto, D. et al.: "A Low-Resistance Self-Aligned T-Shaped Gate for High-Performance Sub-0.1- μm CMOS", IEEE Transactions on Electron Devices, Vol. 44, No. 6, June 1997, pp. 951-956
EXAMINER		DATE CONSIDERED



FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEINFORMATION DISCLOSURE
STATEMENT BY APPLICANT
(37 CFR 1.98(b))

Attorney Docket No.: P2001,0216

Appl. No.:

Applicant: ANNALISA CAPPELLANI ET
AL.

Filing Date: September 26, 2003

Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
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FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
	J						
	K						
	L						
	M						
	N						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

Kasai, K. et al.: "W/WNx/Poly-Si Gate Technology for Future High Speed Deep
Submicron CMOS LSIs", IEEE, 1994, pp. 497-500

EXAMINER

DATE CONSIDERED

EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 63044768
PUBLICATION DATE : 25-02-88

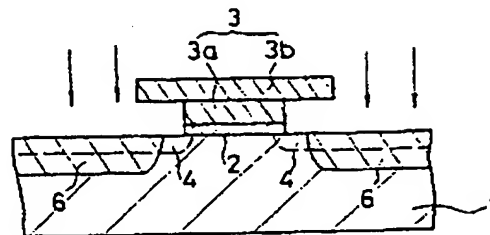
APPLICATION DATE : 12-08-86
APPLICATION NUMBER : 61188815

APPLICANT : MITSUBISHI ELECTRIC CORP;

INVENTOR : SATO SHINICHI;

INT.CL. : H01L 29/78

TITLE : FIELD EFFECT TRANSISTOR AND
MANUFACTURE OF THE SAME



ABSTRACT : PURPOSE: To neutralize a negative potential by a positive voltage applied to a gate electrode even if hot electrons are trapped by an insulating film by a method wherein a gate electrode of a T-shape cross-section is formed on a required part of a substrate and the insulating film is buried between the part of the gate electrode close to the substrate surface and the substrate surface beneath the electrode.

CONSTITUTION: After a gate insulating film 2 is formed on a silicon substrate 1, the material for a gate electrode 3 is applied. The gate electrode material is a double-layer film composed of, for instance, a polycrystalline silicon layer 3a and a high melting point metal layer 3b. By applying plasma etching to the electrode materials 3a and 3b with optimized conditions such as gas composition, gas pressure and electric power, a gate electrode 3 of a T-shape cross-section which has a brim part is formed. Then low concentration diffused layers 4 are provided closer to the gate electrode than high concentration diffused layers 6 and those two type diffused layers form continuous double-layer structures. With this constitution, a highly reliable transistor in which creation of hot carriers is suppressed and the gm deterioration caused by the carriers trapped by the insulating film is avoided can be obtained.

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